withdrawal of the rejection of the claims under the judicially created doctrine of obviousness-type double patenting.

The Office Action rejects claims 1-12, 15-34, 39-47 and 50-58 under 35 U.S.C. § 102, or in the alternative under 35 U.S.C. § 103 over Chen (USP 5,714,766). This rejection is respectfully traversed.

Claim 1 recites a memory device which includes an lamination structure having an energy band profile that is changeable between a first configuration in which a barrier height of the energy band profile is high and a second configuration in which the barrier height of the energy band profile is low, an electric current flowing in the second configuration from the electrode structure to the charge storing node and vice versa in response to given voltages applied to the device so as to charge and discharge the node selectively through the lamination structure. It is respectfully submitted that Chen does not disclose or suggest this feature, and in particular does not disclose or suggest that the node is selectively charged and discharged through the lamination structure, wherein charges are stored on the node in the first configuration, as further explained below.

Chen discloses a memory device in which current flowing in a channel 26 extending between source and drain regions 14 and 18 is influenced by charge held by nanocrystals in layer 34 that acts as a gate overlying the channel. The nanocrystal in region 34 is separated from the channel by a barrier or a injection layer 30. The charge is stored in the nanocrystal in layer 34 by applying a voltage to the control gate 16 that is separated from nanocrystal layer 34 by a relatively thick insulating layer 38. However, as shown in Figs. 3 and 4, the charging and discharging of the nanocrystals 34 occurs through the injection layer 30 to and from the channel 26. There is no charging and discharging to or from the control gate 16 through the insulating spacer layer 41. In this regard, it is noted that the spacer layer 41 is relatively thick in order to provide a large barrier 42, 52 shown in Figs. 3 and 4. This barrier needs to be thick to prevent charge transferred to or from the control electrode 16 so that charge 51 can be stored satisfactory in the potential well formed at the nanocrystal in layer 34. If charge transfer did occur to the control gate 16, the device would not work satisfactorily, because charge could not be held in the potential well at the nanocrystal in layer 34. Thus, in Chen, no significant current flows between the nanocrystal in layer 34 and the control gate 16.

This is further explained at column 6, lines 59-61, where it is indicated that one or a certain number of electrons or holes tunnels through barriers 30 into or out of nanocrystal 34 of storage device 72. The electrons do not tunnel through layer 38 as suggested in the Office Action.

In contrast, the present invention works in a completely different way. According to the specification, current flows from the overlying control gate to the floating gate or memory node when it is desired to charge or discharge the memory node. For example, referring to Fig. 1 of the application, the memory node overlies a source drain path and is separated by a barrier structure 2 from an overlying electrode structure X which acts as a control gate. The height of the electrostatic barrier provided by barrier structure 2 is lowered to enable a current to flow between the memory node 1 and the control electrode X. Thus, in accordance with the invention, memory node 1 is either charged or discharged by current flowing between the electrode structure X and the memory node. In the first configuration, barrier structure 2 provides a relatively high barrier and hence stores charge from the memory node 1. However, when the barrier structure is subject to an applied voltage, the barrier height is reduced to a second configuration enabling charge either to become stored on the memory node 1 or discharged from it. The current flow is to or from the control electrode X and not from the underlying channel of the device in the manner described in Chen.

Referring back to independent claim 1 of the application, Chen does not disclose or suggest the second configuration in which electric currents flows from the electrode structure to the charge storage node and vice versa in response to given voltages applied to the device so as to charge and discharge the node selectively through the lamination structure. Further, it would not be obvious to modify Chen to include flow of electrons from the control gate to the nanocrystals as Chen would not then function for its intended purpose. Accordingly, claim 1 is not obvious or anticipated by Chen.

Each of the other independent claims 3, 5, 15, 21, 35, 45, 50 and 56-58 all contain similar recitations regarding the second configuration as discussed above regarding claim 1. These claims are not anticipated by or obvious over Chen for the same reasons discussed above. Withdrawal of the rejection is requested.

For at least the above reasons, it is submitted that the application is in condition for allowance. Prompt consideration and allowance are solicited.

Attached hereto is a marked up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with Markings to Show Changes Made"**.

The Office is authorized to charge any fees due under 37 C.F.R. § 1.16 or 1.17 to Deposit Account No. 11-0600.

Should there be any questions concerning this matter, the Examiner is invited to contact Applicants undersigned attorney.

Respectfully submitted,

Dated: November 19, 2002

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DCO 432663 v1

APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Page 1, between lines 5 and 6, please insert the following:

This application is a Continuation Application of Application Serial No. 08/958,845, filed October 28, 1997, now U.S. Patent No. 5,952,692.